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| LI, AIMEE J | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/813,599 | WU ET AL. | |
| | Examiner | Art Unit | |
| | Aimee J. Li | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20 and 24* is/are pending in the application.

4a) Of the above claim(s) *24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-20 and new claim 24 have been considered. Claims 1, 9, 12, and 13 have been amended as per Applicant's request. New claim 24 has been added as per Applicant's request.

### *Papers Submitted*

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as filed 09 April 2007; Extension of time for 1 Month as filed 09 April 2007; and Amendment as filed 09 April 2007.

### *Specification*

3. The amendment filed 09 April 2007 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: the language has been amended from reciting "shared execution code" to "cascading execution code". The terms "shared" and "cascading" have significantly different meanings in the art. The Examiner is unsure where support for changing the terminology from "shared" to "cascading" is supported in the original specification and there were no clear arguments that stated and supported that this change in terminology is not new matter. Applicant is required to cancel the new matter in the reply to this Office Action.

### *Election/Restrictions*

4. Newly submitted claim 24 is directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: The original claims 1-20, even as amended, are written in the format of AB(broad) describing a stack based system which uses

cascading execution code in general. The newly added claim 24 is written in the format of B(narrow) describing the specific details of "cascading execution code" as termed by Applicant. Newly added claim 24's details are not necessary for the execution of the original claims 1-20 and are applicable separately to any program code which wishes to use the "cascading execution code" technique, not just that claimed in claims 1-20. As such, claim 24 is subject to restriction due to the separate applicability and detailed searching.

5. Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claim 24 is withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 1-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Please see the new matter objection to the specification above for further explanation.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindwer, U.S. Patent Number 6,298,434 (herein referred to as Lindwer) in view of Raz et al., U.S. Patent Number 6,606,743 (herein referred to as Raz) and in further view of Chan et al., U.S. Patent Number 5,734,908 (herein referred to as Chan).

10. Referring to claim 1, Lindwer has taught a method to execute an instruction on an operand stack, the method comprising:

a. Performing a stack-state-aware translation of the instruction to code to determine an operand stack state for the instruction (Lindwer column 11, lines 3-22) (the preprocessor moves items from registers to memory and adjusts the SP for the instructions);

b. Dispatching the instruction according to the operand stack state for the instruction (inherent); and

c. Executing the instruction (inherent).

11. Lindwer has not taught his translation including determining an entry point into execution code based on the stack state. Raz has taught a language accelerator that uses memory-mapped registers as a stack (Raz column 4, lines 7-12) among other aspects (Raz column 1, line 60 to column 2, line 10). Raz's accelerator translates foreign code to native code and uses memory instructions to implement the stack operations on the memory-mapped stack (Raz column 6, lines 33-38). Thus, the stack state will determine what instructions are used to implement stack operations (e.g. an increment instruction will only pop 1 operand, while an add instruction would

pop two, etc.). This, in turn, will affect the overall code length, thus affecting the entry point of the shared code (Raz column 6, lines 24-51, emphasis on lines 45-51) and the code is threaded (Raz column 4, lines 29-31). The implementation and advantages of multithreading is well known in the art and would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention. Raz states that his method increases the speed at which Java code is executed (Raz column 2, lines 11-12). In addition, Raz's method can be readily implemented in any processor (Raz column 13-1 9), while Lindwer's cannot. Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention to implement Lindwer's stack system as in Raz's to be able to execute Java code faster and to be able to implement the method in any processor.

12. In addition, Lindwer has not taught cascading execution code, wherein said cascading execution code comprises a plurality of tiers of execution code which are enterable at any tier, each tier comprising at least one computer-executable instruction, and wherein the execution comprises entering the cascading code at an entry tier indicated by the determined entry point and executing the entry tier and at least one tier below the entry tier. Chan has taught

a. Cascading execution code (Chan Abstract "...The system operates by selecting from the source code representation a basic block pair comprising a source basic block and one or more target basic block..."; column 1, lines 36-48 "...The invention operates by selecting from the source code representation a basic block pair comprising a source basic block and one or more target basic blocks..."; column 4, line 64 to column 5, line 25 "...Multiple basic blocks are circular an thus eligible for instruction movement if one of the basic blocks (which becomes

the source basic block) always executes after the other basic block or another basic block via a control loop (these become target basic blocks)..."; column 12, lines 31-59 "...a source BB **904**, and a basic block **906**..."; Figure 3; Figure 9A-9C; and Figure 10A-10B – In regards to Chan, the basic blocks are cascaded because once the entry basic block is executed at least one of the following, lower basic blocks are executed.),

b. Wherein said cascading execution code comprises a plurality of tiers of execution code which are enterable at any tier (Chan Abstract "...The system operates by selecting from the source code representation a basic block pair comprising a source basic block and one or more target basic block..."; column 1, lines 36-48 "...The invention operates by selecting from the source code representation a basic block pair comprising a source basic block and one or more target basic blocks..."; column 4, line 64 to column 5, line 25 "...Multiple basic blocks are circular an thus eligible for instruction movement if one of the basic blocks (which becomes the source basic block) always executes after the other basic block or another basic block via a control loop (these become target basic blocks)..."; column 12, lines 31-59 "...a source BB **904**, and a basic block **906**..."; Figure 3; Figure 9A-9C; and Figure 10A-10B – In regards to Chan, the basic blocks are each tier.),

c. Each tier comprising at least one computer-executable instruction (Chan Abstract "...The system operates by selecting from the source code representation a basic block pair comprising a source basic block and one or more target basic block...";

column 1, lines 36-48 "...The invention operates by selecting from the source code representation a basic block pair comprising a source basic block and one or more target basic blocks..."; column 4, line 64 to column 5, line 25 "...Multiple basic blocks are circular an thus eligible for instruction movement if one of the basic blocks (which becomes the source basic block) always executes after the other basic block or another basic block via a control loop (these become target basic blocks)..."; column 12, lines 31-59 "...a source BB **904**, and a basic block **906**..."; Figure 3; Figure 9A-9C; and Figure 10A-10B), and

d. Wherein the execution comprises entering the cascading code at an entry tier indicated by the determined entry point and executing the entry tier and at least one tier below the entry tier (Chan Abstract "...The system operates by selecting from the source code representation a basic block pair comprising a source basic block and one or more target basic block..."; column 1, lines 36-48 "...The invention operates by selecting from the source code representation a basic block pair comprising a source basic block and one or more target basic blocks..."; column 4, line 64 to column 5, line 25 "...Multiple basic blocks are circular an thus eligible for instruction movement if one of the basic blocks (which becomes the source basic block) always executes after the other basic block or another basic block via a control loop (these become target basic blocks)..."; column 12, lines 31-59 "...a source BB **904**, and a basic block **906**..."; Figure 3; Figure 9A-9C; and Figure 10A-10B – In regards to Chan, the basic blocks are cascaded

because once the entry basic block is executed at least one of the following, lower basic blocks are executed.).

**13.** A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Chan, that the basic blocks more fully utilize processor resources (Chan column 1, lines 24-33 "...a software compiler that synthesizes code that more fully utilizes the resources..."). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the basic block tiers of Chan in the device of Lindwer to improve resource utilization.

14. Referring to claim 2, Lindwer in view of Raz and in further view of Chan has taught the method according to claim 1, said performing comprising:

a. Determining a number of operands on the operand stack before the instruction is executed (Lindwer column 11, lines 3-22) (It is inherent that this step will be taken in moving items from registers to memory and adjusting the SP for the instructions);

b. Determining a number of operands on the operand stack after the instruction is executed based on a number of operands that the instruction consumes and a number of operands that the instruction produces (Linder column 11, lines 3-22); and

c. Inferring a number of shift operations required after execution of the instruction to maintain top-of-stack elements (Linder column 11, lines 3-22)

15. Referring to claim 3, Lindwer in view of Raz and in further view of Chan has taught the method according to claim 2, wherein the number of shift operations required after execution of

the instruction is based on the number of operands on the operand stack before the instruction is executed and the number of operands on the operand stack after the instruction is executed (Lindwer column 11, lines 15-22).

16. Referring to claim 4, Lindwer in view of Raz and in further view of Chan has taught the method according to claim 2, wherein the number of shift operations required after execution of the instruction is inferred based on a static lookup table (Lindwer column 6, lines 39-47) (The translation is based on a static table. Through the table, it is known how many operands will be used and how many will be placed back on the stack, and based on that is how many items are transferred to memory.).

17. Referring to claim 5, Lindwer in view of Raz and in further view of Chan has taught the method according to claim 1, wherein the operand stack is a mixed-register stack (Lindwer column 11, lines 15-22).

18. Referring to claim 6, Lindwer in view of Raz and in further view of Chan has taught the method according to claim 1, wherein the operand stack state comprises a number of shift operations to maintain top-of-stack elements of the operand stack after the execution of the instruction (Lindwer column 11, lines 15-22).

19. Referring to claim 7, Lindwer in view of Raz and in further view of Chan has taught the method according to claim 6, wherein the top-of-stack elements comprise a register stack (Lindwer column 11, lines 15-22).

20. Referring to claim 8, Lindwer in view of Raz and in further view of Chan has taught the method according to claim 1, further comprising refilling the operand stack (Linder column 11,

lines 15-22) (The items are moved based on what will be overwritten, meaning that values pushed on the stack from the routine will refill the register part of the stack.).

21. Referring to claim 9, Lindwer has taught a system comprising:

a. An operand stack to execute an instruction (Linder column 11, lines 3-5); and

b. An interpreter to determine a state of the operand stack, translate the instruction into threaded code, and dispatch the instruction based on the state of the operand stack (Linder column 11, lines 3-22) (the preprocessor is the interpreter).

22. Lindwer does not teach his interpreter determining an entry point into execution code based on the stack state. Raz teaches a language accelerator that uses memory-mapped registers as a stack (Raz column 4, lines 7-12) among other aspects (Raz column 1, line 60 to column 2, line 10). Raz's accelerator translates Java code, in some embodiments, to native code and uses memory instructions implement the stack operations on the memory-mapped stack (Raz column 6, lines 33-38). Thus, the stack state will determine what instructions are used to implement stack operations (e.g. an increment instruction will only pop 1 operand, while an add instruction would pop two, etc.). This, in turn, will affect the overall code length, thus affecting the entry point of the shared code (Raz column 6, lines 24-51, emphasis on lines 45-51) and the code is threaded (Raz column 4, lines 29-31). The implementation and advantages of multithreading is well known in the art and would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention. Raz states that his method increases the speed at which Java code is executed (Raz column 2, lines 11-12). In addition, Raz's method can be readily implemented in any processor (Raz column 13-1 9), while Lindwer's cannot. Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's

invention to implement Lindwer's stack system as in Raz's to be able to execute Java code faster and to be able to implement the method in any processor.

23. In addition, Lindwer has not taught cascading execution code. Chan has taught cascading execution code (Chan Abstract "...The system operates by selecting from the source code representation a basic block pair comprising a source basic block and one or more target basic block..."; column 1, lines 36-48 "...The invention operates by selecting from the source code representation a basic block pair comprising a source basic block and one or more target basic blocks..."; column 4, line 64 to column 5, line 25 "...Multiple basic blocks are circular an thus eligible for instruction movement if one of the basic blocks (which becomes the source basic block) always executes after the other basic block or another basic block via a control loop (these become target basic blocks)..."; column 12, lines 31-59 "...a source BB **904**, and a basic block **906**..."; Figure 3; Figure 9A-9C; and Figure 10A-10B – In regards to Chan, the basic blocks are cascaded because once the entry basic block is executed at least one of the following, lower basic blocks are executed.). A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Chan, that the basic blocks more fully utilize processor resources (Chan column 1, lines 24-33 "...a software compiler that synthesizes code that more fully utilizes the resources..."). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the basic block tiers of Chan in the device of Lindwer to improve resource utilization.

24. Referring to claim 10, Lindwer in view of Raz and in further view of Chan has taught the system according to claim 9, wherein the operand stack is a mixed stack comprising a register stack and a memory stack (Linder column 11, lines 15-22).

25. Referring to claim 11, Lindwer in view of Raz and in further view of Chan has taught the system according to claim 10, wherein the register stack comprises at least one register to hold at least one respective top element of the stack and the memory stack comprises a contiguous memory region to hold the remaining elements of the operand stack (Linder column 3, lines 15-22).

26. Referring to claim 12, Lindwer has taught a machine accessible medium containing program instructions that, when executed by a processor, cause the processor to perform a series of operations comprising:

a. Translating a virtual machine instruction into threaded code based on an operand stack state of the virtual machine instruction (Linder column 11, lines 3-22);

b. Dispatching the virtual machine instruction according to the operand stack state (inherent); and

c. Executing the instruction (inherent).

27. Lindwer does not teach his translation including determining an entry point into execution code based on the stack state. Raz teaches a language accelerator that uses memory-mapped registers as a stack (Raz column 4, lines 7-12) among other aspects (Raz column 1, line 60 to column 2, line 10). Raz's accelerator translates Java code, in some embodiments, to native code and uses memory instructions implement the stack operations on the memory-mapped stack (Raz column 6, lines 33-38). Thus, the stack state will determine what instructions are used to implement stack operations (e.g., an increment instruction will only pop 1 operand, while an add instruction would pop two, etc.). This, in turn, will affect the overall code length, thus affecting the entry point of the shared code (Raz column 6, lines 24-51, emphasis on lines 45-51) and the

code is threaded (Raz column 4, lines 29-31). The implementation and advantages of multithreading is well known in the art and would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention. Raz states that his method increases the speed at which Java code is executed (Raz column 2, lines 11-12). In addition, Raz's method can be readily implemented in any processor (Raz column 13-1 9), while Lindwer's cannot. Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention to implement Lindwer's stack system as in Raz's to be able to execute Java code faster and to be able to implement the method in any processor.

28. In addition, Lindwer has not taught cascading execution code, wherein said cascading execution code comprises a plurality of tiers of execution code which are enterable at any tier, and each tier comprising at least one computer-executable instruction. Chan has taught

a. Cascading execution code (Chan Abstract "...The system operates by selecting from the source code representation a basic block pair comprising a source basic block and one or more target basic block..."; column 1, lines 36-48 "...The invention operates by selecting from the source code representation a basic block pair comprising a source basic block and one or more target basic blocks..."; column 4, line 64 to column 5, line 25 "...Multiple basic blocks are circular an thus eligible for instruction movement if one of the basic blocks (which becomes the source basic block) always executes after the other basic block or another basic block via a control loop (these become target basic blocks)..."; column 12, lines 31-59 "...a source BB **904**, and a basic block **906**..."; Figure 3; Figure 9A-9C; and Figure 10A-10B – In regards to Chan, the basic blocks are cascaded

because once the entry basic block is executed at least one of the following, lower basic blocks are executed.),

b. Wherein said cascading execution code comprises a plurality of tiers of execution code which are enterable at any tier (Chan Abstract "...The system operates by selecting from the source code representation a basic block pair comprising a source basic block and one or more target basic block..."; column 1, lines 36-48 "...The invention operates by selecting from the source code representation a basic block pair comprising a source basic block and one or more target basic blocks..."; column 4, line 64 to column 5, line 25 "...Multiple basic blocks are circular an thus eligible for instruction movement if one of the basic blocks (which becomes the source basic block) always executes after the other basic block or another basic block via a control loop (these become target basic blocks)..."; column 12, lines 31-59 "...a source BB **904**, and a basic block **906**..."; Figure 3; Figure 9A-9C; and Figure 10A-10B – In regards to Chan, the basic blocks are each tier.), and

c. Each tier comprising at least one computer-executable instruction (Chan Abstract "...The system operates by selecting from the source code representation a basic block pair comprising a source basic block and one or more target basic block..."; column 1, lines 36-48 "...The invention operates by selecting from the source code representation a basic block pair comprising a source basic block and one or more target basic blocks..."; column 4, line 64 to column 5, line 25 "...Multiple basic blocks are circular an thus eligible for instruction movement if one of the

basic blocks (which becomes the source basic block) always executes after the other basic block or another basic block via a control loop (these become target basic blocks)..."; column 12, lines 31-59 "...a source BB **904**, and a basic block **906**..."; Figure 3; Figure 9A-9C; and Figure 10A-10B).

29. A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Chan, that the basic blocks more fully utilize processor resources (Chan column 1, lines 24-33 "...a software compiler that synthesizes code that more fully utilizes the resources..."). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the basic block tiers of Chan in the device of Lindwer to improve resource utilization.

30. Referring to claim 13, Lindwer in view of Raz and in further view of Chan has the machine accessible medium according to claim 12, wherein the threaded code is based on an entry point into cascading execution code (Linder column 11, lines 3-22) (it is an entry into a subroutine) (Raz column 6, lines 45-51).

31. Referring to claim 14, Lindwer in view of Raz and in further view of Chan has the machine accessible medium according to claim 12, further containing program instructions that, when executed by the processor cause the processor to perform further operations comprising:

a. Determining a number of operands that are present on an operand stack at a time before the virtual machine instruction is executed (Linder column 11, lines 3-22) (It is inherent that this step will be taken in moving items from registers to memory and adjusting the SP for the instructions);

b. Determining a number of operands that are present on the operand stack at a time after the virtual machine instruction is executed (Linder column 3, lines 3-22); and

c. Inferring a number of shift operations required to maintain top-of-stack elements after the virtual machine instruction is executed (Linder column 3, lines 3-22).

32. Referring to claim 15, Lindwer in view of Raz and in further view of Chan has the machine accessible medium according to claim 13, wherein the wherein the number of shift operations required after execution of the instruction is based on the number of operands present on the operand stack at a time before the instruction is executed and the number of operands present on the operand stack at a time after the instruction is executed (Linder column 11, lines 15-22).

33. Referring to claim 16, Lindwer in view of Raz and in further view of Chan has the machine accessible medium according to claim 13, wherein the number of shift operations required after execution of the instruction is inferred based on a static lookup table (Linder column 6, lines 39-47) (The translation is based on a static table. Through the table, it is known how many operands will be used and how many will be placed back on the stack, and based on that is how many items are transferred to memory.).

34. Referring to claim 17, Lindwer in view of Raz and in further view of Chan has the machine accessible medium according to claim 12, wherein the operand stack state comprises a number of shift operations to maintain top-of-stack elements of an operand stack after execution of the virtual machine instruction (Linder column 11, lines 15-22).

35. Referring to claim 18, Lindwer in view of Raz and in further view of Chan has the machine accessible medium according to claim 17, wherein the top-of-stack elements comprise a register stack (Linder column 11, lines 15-22).

36. Referring to claim19, Lindwer in view of Raz and in further view of Chan has the machine accessible medium according to claim 12, further containing program instructions that, when executed by the processor cause the processor to perform further operations comprising execute a number of shift operations to replace top-of-stack elements to an operand stack (Linder column 11, lines 15-22) (The items are moved based on what will be overwritten, meaning that values pushed on the stack from the routine will refill the register part of the stack.).

37. Referring to claim 20, Lindwer in view of Raz and in further view of Chan has the machine accessible medium according to claim 19, wherein the number of shift operations is based on a number of elements on the operand stack that are consumed by the virtual machine instruction and a number of elements that are produced by the virtual machine instruction (Linder column 11, lines 15-22) (The items are moved based on what will be overwritten, meaning that values pushed on the stack from the routine will refill the register part of the stack.).

***Response to Arguments***

38. Applicant's arguments with respect to claims 1-20 and 24 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

39. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of

claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Emma et al., U.S. Patent Number 5,333,283, has taught multi-way or switch handling.

b. Steele, Jr., U.S. Patent Number 5,903,899, has taught stack-based program execution with an operand stack to store operand data.

c. Cartwright, Jr., U.S. Patent Number 6,075,942, has taught operand-stack-oriented code which store instruction operands on a stack.

d. Luch et al., U.S. Patent Number 6,292,935, has taught an operand stack based code with basic block of codes between branches.

e. Czajkowski et al., U.S. Patent Number 6,993,761, has taught a stack-based system that checks for stack underflows and overflows when instructions are to be executed.

f. Nevill et al., U.S. Patent Number 7,000,094 and U.S. Patent Application Publication 2002/0066004, are the U.S. Patent version of the cited Chinese Patent, and have taught an operand stack based instruction program executing on a register based system.

g. Duesterwald ald, U.S. Patent Application Publication 2003/0192035, has taught stack-based code that maps register values to operand stack values.

h. Bottomley, U.S. Patent Application Publication 2004/0015912, has taught JAVA stack based code that pushes and pops operand arguments onto an operand stack.

40. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

41. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

42. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aimee J. Li

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Examiner
Art Unit 2183

25 May 2007